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	Applicant : Hwu et al.	
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U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation Yes	Translation No

AH	B. R. Rau and C. D. Glaeser, Some Scheduling Techniques and An Easily Schedulable Horizonal Architecture for High Performance Scientific Computing,in *Proceedings of the 20th Annual Workshop on Microprogramming and Microarchitecture*, pp. 183-198, October 1981
AH	J. C. Dehnert, P. Y. Hsu, and J. P Bratt, Overlapped Loop Support in the Cydra 5,in *Proceedings of the 3rd International Conference on Architectural Support for Programming Languages and Operating Systems*, pp. 26-38, April 1989.
AH	TMS320C6000 CPU and Instruction Set Reference Guide,Tech. Rep. SPRU189F, Texas Instruments, Oct. 2000, Chapters 1 and 2.
AH	TMS320C6000 Programmers Guide, Rep. SPRU198G, Texas Instruments, Aug. 2002, pp. 5-32 to 5-149.
AH	M. S. Lam, Software pipelining: An effective scheduling technique for VLIW machines,in *Proceedings of the ACM SIGPLAN 1988 Conference on Programming Language Design and Implementation*, pp. 318-328, June 1988
AH	B. R. Rau, M. S. Schlansker, and P. Tirumalai, Code generation schemas for modulo scheduled do-loops and while-loops,Tech. Rep. HPL-92-47, Hewlett Packard Labs, April 1992
AH	D. M. Lavery, *Modulo Scheduling for Control-Intensive General-Purpose Programs*. Ph.D. thesis, Department of Electrical and Computer Engineering, University of Illinois, Urbana, IL, 1997

EXAMINER Aimee Li	DATE CONSIDERED 10/15/2004

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.